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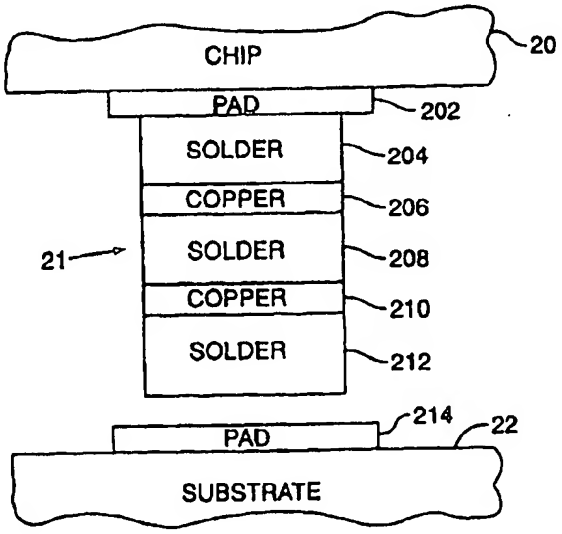
(54) Title: MULTILAYER SOLDER/BARRIER ATTACH FOR SEMICONDUCTOR CHIP



(57) Abstract

A multilayer attach (21) including alternating layer of solder (204, 208, 212) and barrier metals (206, 210) is used to replace the conventional solder bumps or balls in flip-chip bonding. The thin solder layers undergo grain boundary sliding deformation rather than matrix deformation when the attach is subjected to lateral shear forces as a result of the differential thermal expansion of the chip (20) and the substrate (22). Grain boundary sliding deformation is relatively damage-free as compared to matrix deformation, which generates voids, cracks and fractures in the attach, ultimately leading to a defective electrical or thermal connection. In one embodiment, the attach includes three solder layers each of which is no more than 50 μm thick.

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MULTILAYER SOLDER/BARRIER ATTACH FOR SEMICONDUCTOR CHIP

This application claims priority based on Provisional Application No. 60/016,430. filed April 29, 1996.

FIELD OF THE INVENTION

This invention relates to structures and methods of forming an electrical, thermal or mechanical attachment between bodies which have different thermal coefficients of expansion. This invention relates particularly to structures and methods of forming an electrical or thermal attachment between a semiconductor chip or package and a printed circuit board or other substrate.

BACKGROUND OF THE INVENTION

Semiconductor chips are commonly attached to printed circuit boards (PCBs) by arrays of solder bumps or balls. For example, in "flip-chip" bonding an array of solder bumps is formed on the front side of the chip. The chip is then inverted and the solder bumps are heated (reflowed) to form a connection with pads on the PCB. This structure provides a direct electrical connection which reduces noise and parasitics and increases speed as compared with, for example, the use of bonding wires to connect the chip and the PCB. In the fabrication of multichip modules flip-chip bonding allows a better use of the available real estate on the PCB and eliminates the need for a separate chip package. In a similar manner, a ball grid array consisting of solder balls can be used to connect pads on an "interposer" placed between a semiconductor chip and a PCB with pads on the PCB.

The solder bumps employed in flip-chip bonding and ball grid arrays are typically 125-200 mm in diameter and are frequently formed by electroplating or evaporation.

A problem occurs when the chip and PCB (or interposer) are subjected to temperature variations. Because these two bodies normally have different temperature coefficients of expansion, the solder bumps are subjected to shear stresses and exhibit defects after a number of thermal cycles. A silicon chip has a thermal coefficient of expansion (α) of 2.6×10^{-6} in/in/°C while a PCB, for example, has an α of about 16×10^{-6} in/in/°C. For example, in an

array of bumps on a large (> 0.5") die, a C4 solder bump attach bonded to a copper substrate will last only about 100 thermal cycles (-60°C to 150°C).

The problem of differential thermal expansion can be overcome to some extent by adding structural support for the solder bumps by filling the spaces between them with a plastic material (a process known as "underfilling"), but this solution is time-consuming and expensive. It also renders the structure non-repairable.

Ordinary solder bump structures last less than 100 thermal cycles (from -40°C to 125°C). With underfilling this can be increased to about 2500 thermal cycles. Using very large, 250 mm-diameter solder bumps on 500 mm centers increases the lifetime of the bumps to about 1000 thermal cycles. This solution, however, consumes an excessive amount of space, and the resulting electrical connections are slower and noisier than is desirable.

Accordingly, there is a clear need for an economical technique of increasing the thermal lifetime of direct electrical connections between a semiconductor chip or an interposer and an underlying substrate such as a PCB.

SUMMARY OF THE INVENTION

According to this invention, a connection between a first body such as a semiconductor chip and a second body such as a PCB is formed by a multilayer structure or stack which includes solder layers interleaved with barrier layers. The solder layers are made sufficiently thin that a grain boundary sliding form of deformation occurs when the first and second bodies thermally expand or contract at different rates. Grain boundary sliding predominates when the solder is finely grained and is distinguishable from matrix deformation, which occurs when the grains of solder are relatively large. Grain boundary sliding is damage-free and reversible, whereas matrix deformation is irreversible. Matrix deformation permanently damages the granular structure of the solder and ultimately impairs the integrity of the electrical connection.

Making the solder layers thin creates a thin granular structure and promotes grain boundary sliding. In addition, the thinness of the solder layers restrains grain growth during thermal cycling, resulting in a stable fine-grained structure.

In one group of embodiments the solder layers are less than 50 mm thick and there are at least three solder layers in the stack. The solder layers are separated by barrier layers which can include one or more layers or sublayers of Ni, Cu, Co, Pd, Pt or Ru. The stack of solder and barrier layers is fabricated by electroplating . Small sizes and shapes of the connections can be defined using photolithographic processes.

The applicability of this invention extends far beyond the formation of an array of electrical connections between the respective pads on semiconductor chips (or interposers) and PCBs. This invention can also be used, for example, as a means of attaching a broader area of a semiconductor chip to a heat sink.

The use of this invention provides dramatically increased thermal lifetimes. Replacing a conventional solder bump with a stack containing three solder layers increases the estimated lifetime of the connection from 100 to 2500 thermal cycles. If the number of solder layers is increased to five, the estimated lifetime increases to 5000 thermal cycles or more.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B illustrate top and side views, respectively, of an array of attach bumps in accordance with this invention.

Fig. 1C illustrates a detailed view of one of the attach bumps.

Fig. 2A illustrates a side view of an attach bump containing three solder layers before reflow.

Fig. 2B illustrates a side view of the attach bump of Fig. 2A after reflow.

Fig. 3 illustrates a graph of the shear force versus strain rate for matrix deformation and for grain boundary sliding deformation in thick and thin solder layers.

Fig. 4 illustrates a graph of the strain rate corresponding to the "knee" (shown in Fig. 3) as a function of the thickness of the solder layer.

Fig. 5 illustrates a graph of the lifetime of a multilayer attach (in thermal cycles) as a function of the number of solder layers in the stack for solder layers of various thickness.

Fig. 6 is a detailed side view of an attach bump of this invention containing three solder layers.

Fig. 7 is a detailed side view of an attach bump of this invention containing two solder layers.

Fig. 8 is a side view of an embodiment containing multilayer attach bumps in series with conventional solder balls.

DESCRIPTION OF THE INVENTION

Figs. 1A and 1B are top and side views, respectively, of a semiconductor chip 10 which contains an array of multilayer attach bumps 12 in accordance with this invention. Fig. 1C is a detailed view of one of the attach bumps 12, which includes a solder layer 13, a Ni/Cu

barrier layer 14 and a solder layer 15. Solder layer 15 is in electrical contact with a metal bus 16 on the surface of the chip 10. (Note that Fig. 1C is not drawn to scale.) Thus bump 12 contains two solder layers and an intervening barrier layer.

Figs. 2A and 2B show an attach bump 21 containing three solder layers that is formed on a pad 202 of a semiconductor chip 20. Attach bump 21 includes solder layers 204, 208, 212 and intervening copper layers 206, 210. In Fig. 2A, attach bump 21 has not yet been bonded to a pad 214 on substrate 22, which could be, for example, a PCB. Fig. 2B shows attach bump 21 after it has been bonded to pad 214 by reflowing the solder layers 204, 208, 212. Also, as is apparent from Fig. 2B, pad 214 has been displaced laterally with respect to pad 202 as a result of differential thermal expansion between chip 20 and substrate 22. The lateral displacement of solder layers 204, 208, 212 is also apparent.

Each of the solder layers in attach bumps 12 and 21 are preferably less than 50 mm thick. Keeping the solder layers below a thickness of 50 μm insures that the grains in the solder are small and that the predominant form of deformation as the chip and substrate are displaced laterally by temperature variations is grain boundary sliding deformation rather than matrix deformation.

Fig. 3 illustrates a graph showing the lateral shear force applied to the solder as a function of the rate of deformation (strain rate). Curve 30 shows the force vs. strain rate for matrix deformation. Curve 31 shows the force vs. strain rate for grain boundary sliding deformation when the layer is relatively thick (150 μm), and curve 32 shows the force vs. strain rate for grain boundary sliding deformation when the solder layer is relatively thin (50 μm). A "knee" for the "thick" solder layer indicated at 33 represents the intersection of curves 30 and 31, and a "knee" for the "thin" solder layer indicated at 34 represents the intersection of curves 30 and 32. A thin solder layer cools more rapidly than a thick solder layer, resulting in a higher grain boundary density which shifts the knee to higher strain rates.

For example, a differential thermal expansion which produces a shear force of F_1 results in a strain rate of A_1 from grain boundary sliding deformation in a thin solder layer and a strain rate of A_2 from matrix deformation. Since the intersection with curve 32 is below the knee 34, A_2 is almost two orders of magnitude below A_1. Thus the predominant form of deformation in a thin solder layer is grain boundary sliding. In contrast, with a thick solder layer the point at which force F_1 intersects curve 31 (dashed line) yields a strain rate of A_3 for grain boundary sliding deformation. The strain rate for matrix deformation remains at A_2 since

the relationship of strain rate and force for matrix deformation is independent of the thickness of the solder layer. Since the intersection with curve 31 is above knee 33, A_2 is somewhat greater than A_3, and matrix deformation predominates.

Thus it is apparent from Fig. 3 that when the maximum shear force intersects the force vs. strain rate curves *below* the applicable "knee", grain boundary sliding deformation will predominate over matrix deformation, and when the maximum shear force is *above* the applicable "knee", matrix deformation will predominate. Since the "knee" for a thin solder layer is higher than the "knee" for a thick solder layer, grain boundary sliding deformation is more likely to predominate in a thin solder layer.

During a thermal cycle on a 1/2-inch chip (-40°C to 140°C) the maximum strain rate generated may be estimated, which in Fig. 3 is represented by A_1. It is seen that when this strain rate is A_1, the maximum force generated in the thick solder joint is F_2, and the maximum force generated in the thin solder joint is F_1. This translates into a matrix strain rate in the thick solder joint of A_1, and a matrix strain rate in the thin joint of A_2, which is lower by about 1½ orders of magnitude. Since the damage rate is proportional to the maximum matrix rate, this explains the 4/1 lifetime increase for this thermal cycle in the thin solder layers because most of the strain in these joints is generated in the form of grain boundary sliding instead of matrix deformation as is the case for the thick solder joint.

The grains in a thin solder layer are much smaller than those in a thick solder layer, and this explains the predominance of grain boundary sliding deformation in the thin layer. Grain boundary sliding deformation is essentially "damage free". In contrast, matrix deformation generates voids, cracking and ultimate fracture from the dislocation climb process. Moreover, the smaller grains in the thin solder layer recrystalize into small grains during thermal cycling. Grain growth is inhibited. Thus the thin solder layer insures that the grains are small initially and insures that the small grain size is maintained thereby promoting a lower damage rate.

Fig. 4 illustrates a graph showing the experimentally determined location of the "knee" as a function of the thickness of the solder layer. As indicated, the knee shifts upward by 2 to 3 orders of magnitude as the layer thickness decreases from about 200 μm to about 75 μm.

Fig. 5 is a graph showing the lifetime of an attach bump as a function of both the thickness of the solder layers and the number of solder layers in the stack. The lifetime is represented as the number of thermal cycles (-40°C to 140°C) at which failure occurs. For the 175 μm thick layer attach, the lifetime increases only linearly with the number of layers in the

attach, increasing only from 50 to 200 thermal cycles (for a four-layer attach). For a 50 μm layer attach the lifetime increases exponentially from about 125 thermal cycles for a single-layer attach to 750 thermal cycles for 2-layer attach to 2500 thermal cycles for a 3-layer attach to 5000 thermal cycles for a 4-layer attach. Similarly, power law increases in lifetime are found for the 37.5 and 25 μm layer attaches.

The multilayer structure of this invention is fabricated by electroplating a succession of solder and barrier layers. Initially, the locations of the attach bumps can be defined using conventional photolithographic techniques. Fig. 1C, for example, shows a photoresist layer 18 (dashed lines) which is used as a mask to define the location of attach bump 12. It may be necessary also to etch an opening in a passivation layer to expose the metal bus or other metal layer to which the attach bump is to be connected. Alternatively, a multilayer laminate of solder and barrier layers can be plated initially and then etched to form the desired attach bumps.

Referring to Fig. 6, a three solder layer attach bump 60 is formed on a silicon die 61, which is typically part of a silicon wafer. Initially a TiW or TiCr adhesion/barrier layer 62 is sputtered onto the surface of silicon chip 61. Layer 62 can be in the range of 100-500 nm thick. This is followed by sputtering a 500 nm thick copper seed layer 63.

This completes the preliminary processing of the silicon chip 61. Next a 2 μm copper layer 64 is electroplated using a sulfate solution. This is followed by electroplating a 2 μm nickel layer 65 (high tin content solder) and another 2 μm copper layer 66, which is also electroplated using a sulfate solution.

Then a 10-25 μm thick solder layer 67 is electroplated using an acid solution (e.g., sulfonic acid). 60/40 solder is preferred because it exhibits the grain boundary sliding mode of deformation for fine grained structures. A 1 μm thick copper strike or adhesion layer 68 is electroplated using a copper cyanide solution before the next copper layer is plated.

This completes the processing for one solder layer. Next a copper layer 64A, a nickel layer 65A and a copper layer 66A are electroplated. Layers 64A-66A are similar to layers 64-66. This is followed by electroplating a solder layer 67A, which is similar to solder layer 67 and a copper layer 68A, which is similar to copper layer 68. A third solder layer is then formed by electroplating layers 64B-67B which are similar to layers 64-67, respectively.

If a photoresist layer is used to define the attach bump, the photoresist is then removed. Solder layers 67, 67A and 67B are then heated to a temperature in the range of

220°C to reflow the solder. Normally, no sidewalls or other mechanical restraints are needed to confine or support the solder during reflow. This produces a fine-grained solder and improves the intermetallic bonding between the solder and adjacent layers. Next silicon chip 61 is diced from other chips on the wafer. Chip 61 is loaded in a flip-chip bonder and aligned with a metal substrate interconnect 69, which could be a metal pad. Conventional tests are then performed to verify the electrical and mechanical integrity of the connection between silicon chip 61 and metal substrate interconnect 69.

In the structure of Fig. 6, layers 64-66 and 68, 64A-66A and 68A, and 64B, 66B are barrier layers. In this embodiment the barrier layers include copper and nickel layers, but in other embodiments one or more members of the group consisting of Co, Pd, Pt and Ru can be used in the barrier layers in addition to or substitution for the copper and nickel layers. Although a three-layer structure is shown in Fig. 6, other embodiments may include more or less than 3 solder layers. Attach bump 60 shown in Fig. 6 has an estimated lifetime of 2500 thermal cycles.

For example, Fig. 7 shows a two-solder-layer attach bump 70 including a TiW or TiCr layer 72 and a copper seed layer 73 which are electroplated on a silicon chip 71. Layers 72 and 73 are similar to layers 62 and 63 shown in Fig. 6. Similarly, layers 74-77 are similar to layers 74A-77A and correspond to layers 64-67 shown in Fig. 6. The electroplated structure is reflow bonded to a metalized substrate such as metal pad 69. Alternatively, the electroplated structure can be bonded to a leadframe or heat sink. The multilayer attach has an estimated lifetime of 750 thermal cycles.

An attach bump in accordance with this invention can be used in other situations such as the one shown in Fig. 8. There a ceramic chip carrier 81 is connected to metal pads 82 on a PCB 83 via conventional solder ball joints 84 in series with five-layer attach bumps 85. The solder layers in attach bumps 85 are 50 μm thick and are separated by copper or nickel barrier layers. Whereas a single solder layer 150-250 μm thick has an experimental lifetime of only 50 thermal cycles the five-layer attach bumps 85 have a calculated lifetime of at least 5000 thermal cycles.

A multilayer laminate structure containing solder and barrier layers can also be used to attach a chip to, for example, a heat sink. A single thick solder layer (e.g., 100 μm) has poor thermal fatigue resistance when used to connect a semiconductor chip to a copper substrate. By reducing the thickness from 100 μm to 50 μm, the thermal lifetime increases by a factor of

two. Reducing the thickness to 25 μm increases the thermal lifetime by a factor of 4-5. As described above, it is the predominance of grain boundary sliding deformation in thin solder layers that accounts for this four- or fivefold improvement in lifetime.

Moreover, increasing the number of solder layers to 2, 3, or 4 decreases the operating strain rate linearly by a factor of 1/2, 1/3 or 1/4, respectively. The operating strain rate is equal to $\Delta\alpha$ x (½ chip dimension/h) x $\Delta T/\Delta t$, where $\Delta\alpha$ is the difference in the thermal coefficient of expansion between the chip and the substrate, h is the height of the solder joint, and $\Delta T/\Delta t$ is the maximum temperature rate of change. By extrapolating the data it is found that the damage rate (i.e., the maximum matrix strain rate in a thermal cycle) decreases by a power of 3 as the number of solder layers increases. This provides order-of-magnitude increases in the thermal lifetime of the structure.

Multilayer attaches in accordance with this invention can also be used for attaching semiconductor chips to a substrate in chip-on-glass (COG) flat panel displays. This permits a higher density of pixels for better resolution. Construction is simplified at reduced costs, and the robustness of the display is increased.

While specific embodiments according to this invention have been described, it will be understood by those skilled in the art that numerous alternative embodiments are within the scope of this invention.

CLAIMS

I claim:

1. A multilayer attach for forming a connection between a first body and a second body, said attach comprising a plurality of solder layers and a plurality of barrier layers, adjacent ones of said solder layers being separated by at least one of said barrier layers.

2. The multilayer attach of Claim 1 wherein said first body comprises a semiconductor chip.

3. The multilayer attach of Claim 1 wherein each of said solder layers has a thickness of 50 μm or less.

4. The multilayer attach of Claim 3 wherein said barrier layers comprise copper.

5. The multilayer attach of Claim 3 wherein said barrier layers comprise copper and nickel.

6. The multilayer attach of Claim 3 wherein said barrier layers comprise one or more metals selected from the group consisting of Cu, Ni, Co, Pd, Pt and Ru.

7. A combination comprising the multilayer attach of Claim 1 and a first body, said attach being attached to said first body.

8. The combination of Claim 7 wherein said first body comprises a semiconductor chip.

9. The combination of Claim 8 further comprising an adhesion layer interposed between said attach and said first body.

10. The combination of Claim 9 wherein said adhesion layer comprises a material selected from the group which consists of TiW or TiCr.

11. A method of forming an attach bump comprising the steps of:

electroplating a first solder over a semiconductor chip.

elecroplating a first metal barrier layer on said first solder layer; and

electroplating a second solder layer on said metal barrier layer.

12. The method of Claim 11 wherein the step of electroplating a first metal barrier layer comprises electroplating a copper layer.

13. The method of Claim 11 wherein each of the steps of electroplating said first and second solder layers comprises electroplating a solder layer less than 50 μm thick.

14. The method of Claim 11 wherein each of the steps of electroplating said first and second solder layers comprises electroplating a solder layer 10-25 μm thick.

15. The method of Claim 11 wherein each of the steps of electroplating said first and second solder layers comprises electroplating a solder layer using an acid solution.

16. The method of Claim 11 wherein the step of electroplating a first metal barrier layer comprises electroplating a copper layer using a copper cyanide solution.

17. The method of Claim 11 further comprising the step of forming an adhesion/barrier layer between said semiconductor chip and said first solder layer.

18. The method of Claim 17 wherein the step of forming an adhesion/barrier layer comprises forming a layer of a material selected from the group consisting of TiW and TiCr.

19. The method of Claim 11 comprising the further steps of:

electroplating a second metal barrier layer on said second solder layer; and

electroplating a third solder layer on said second metal barrier layer.

20. The method of Claim 19 comprising the further step of reflow bonding said attach bump to a metal conductive layer.

FIG. 1A

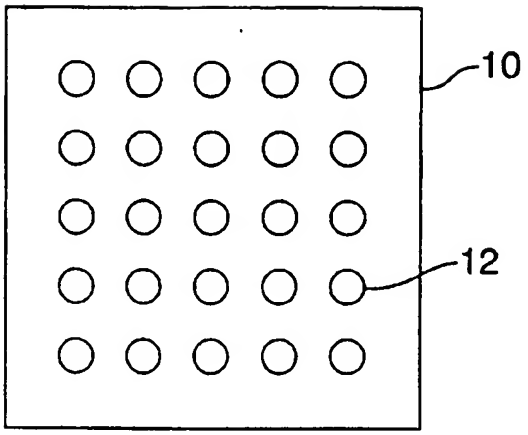


FIG. 1B

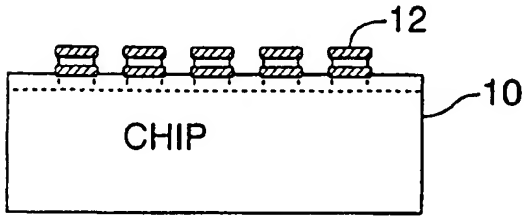


FIG. 1C

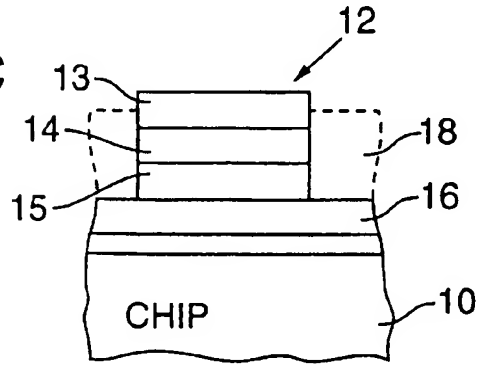
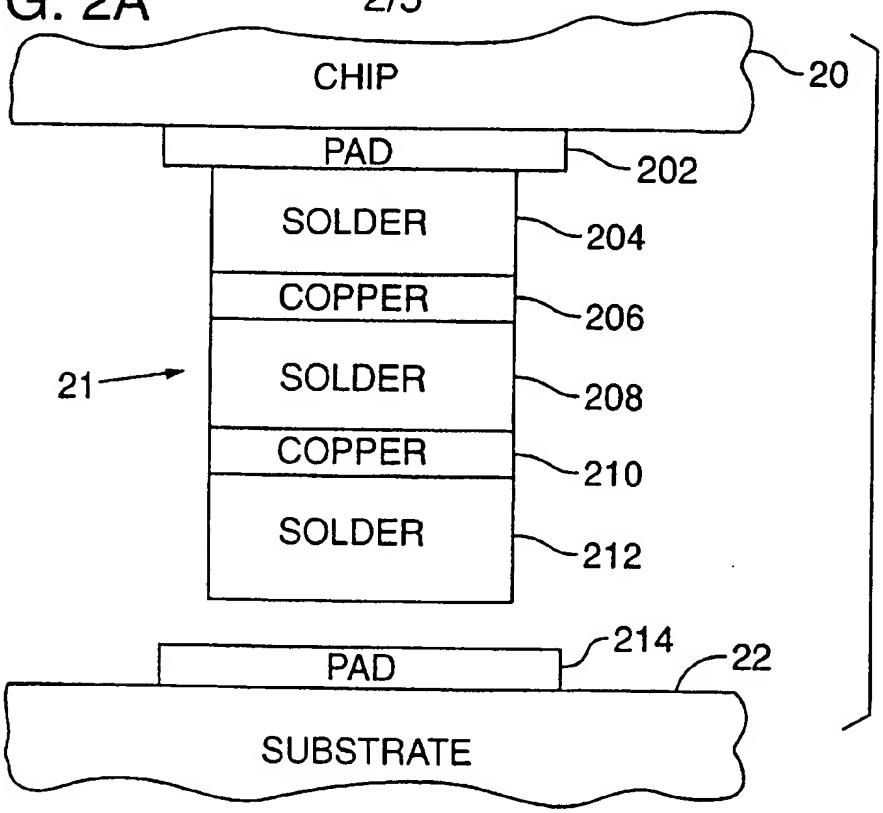


FIG. 2A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PAD
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SOLDER
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21
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208
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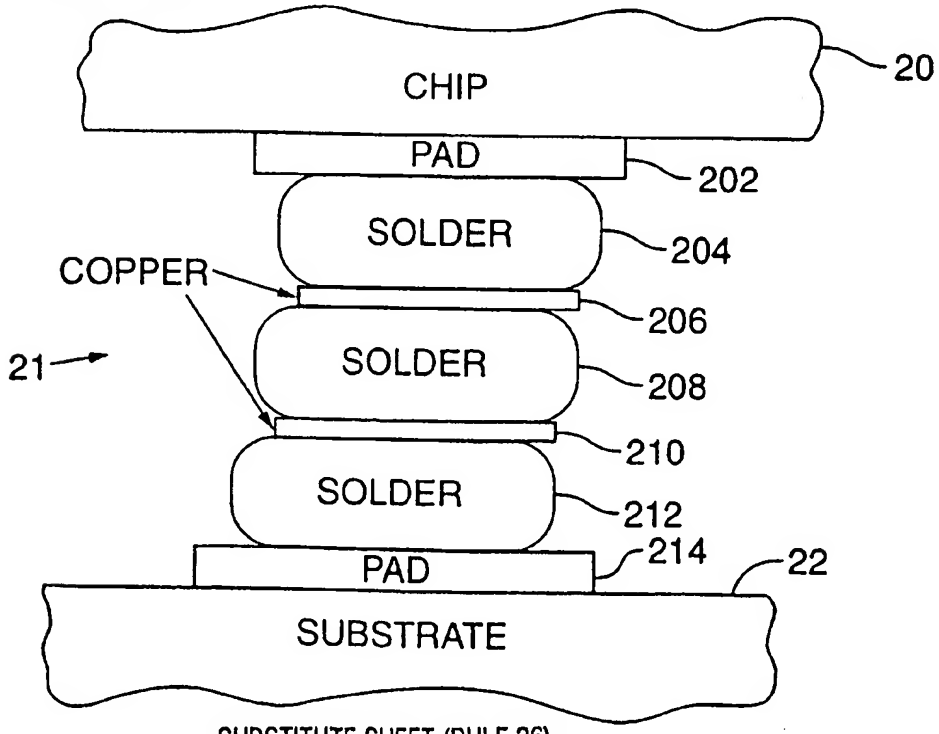
SOLDER
212
214
PAD
22
SUBSTRATE

FIG. 2B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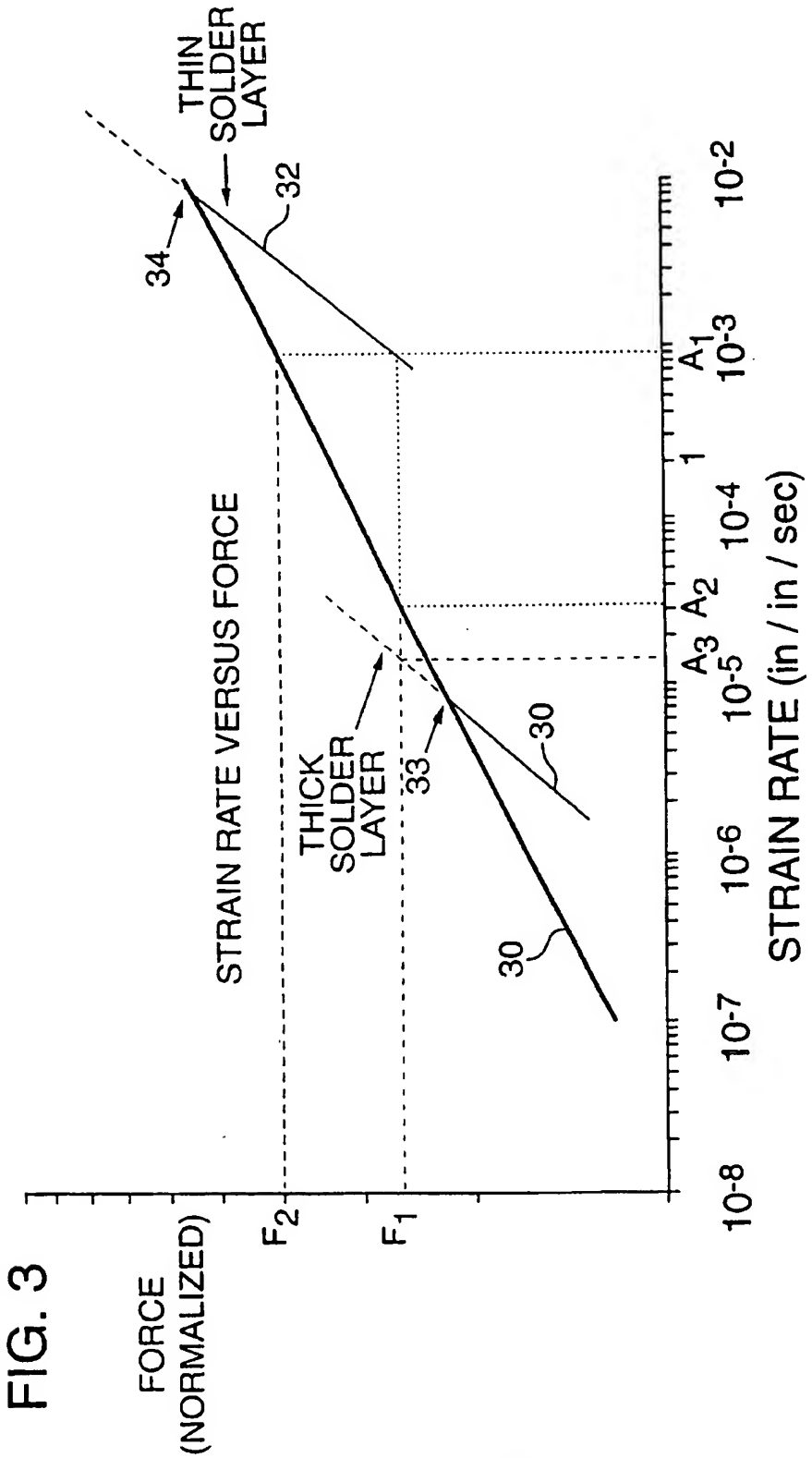
THIN SOLDER LAYER
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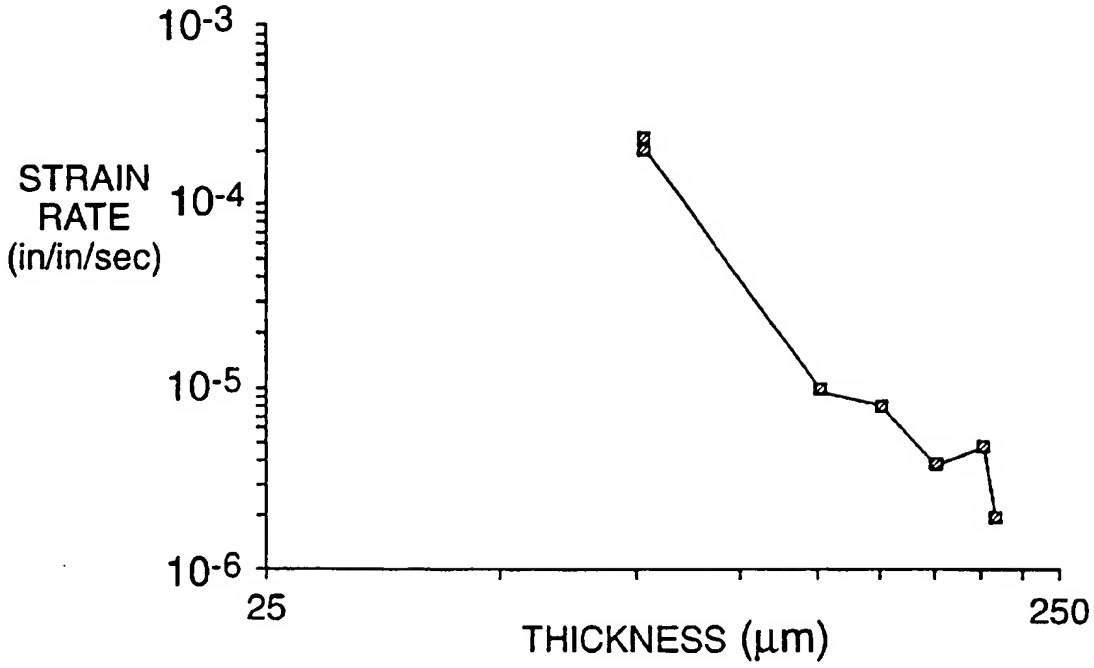
34
STRAIN RATE VERSUS FORCE
THICK SOLDER LAYER
33
30
30
FORCE (NORMALIZED)
F2
F1
A1
A2
A3
10-2
10-3
10-4
10-5
10-6
10-7
10-8
1
STRAIN RATE (in / in / sec)

FIG. 3

FIG. 4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10-5
10-6
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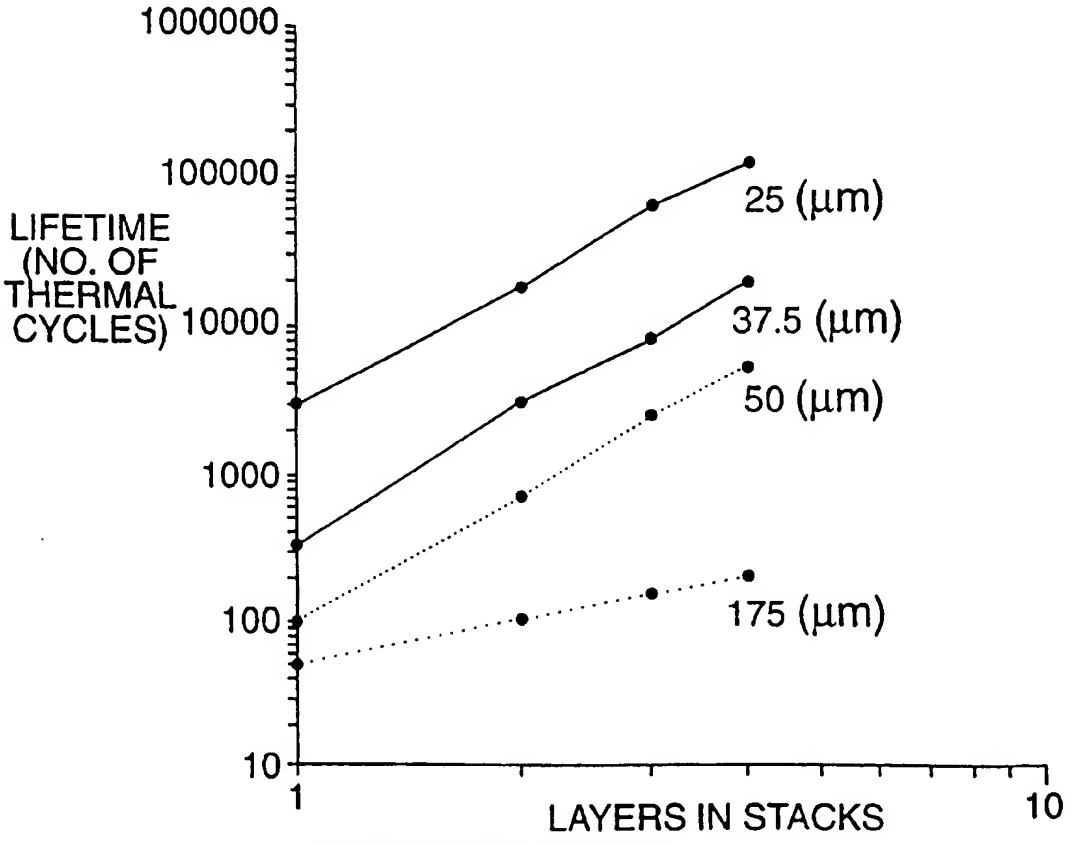
250
THICKNESS (µm)

FIG. 5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10
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10
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50 (µm)
175 (µm)

FIG. 6

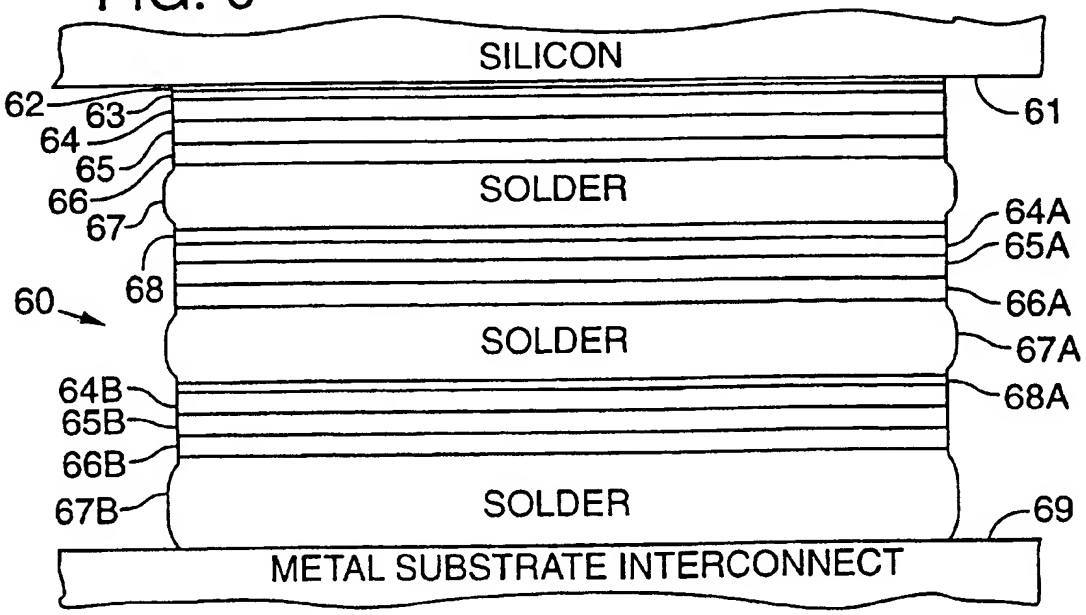


FIG. 7

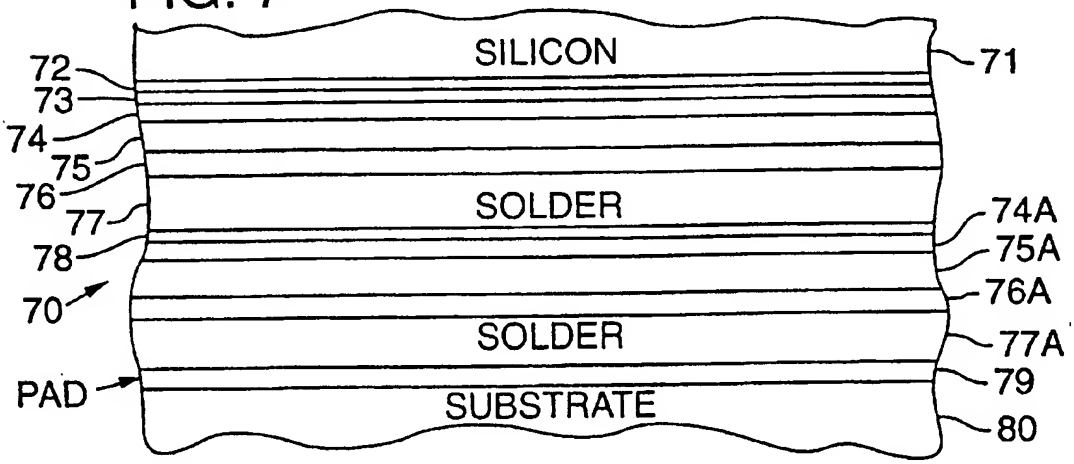
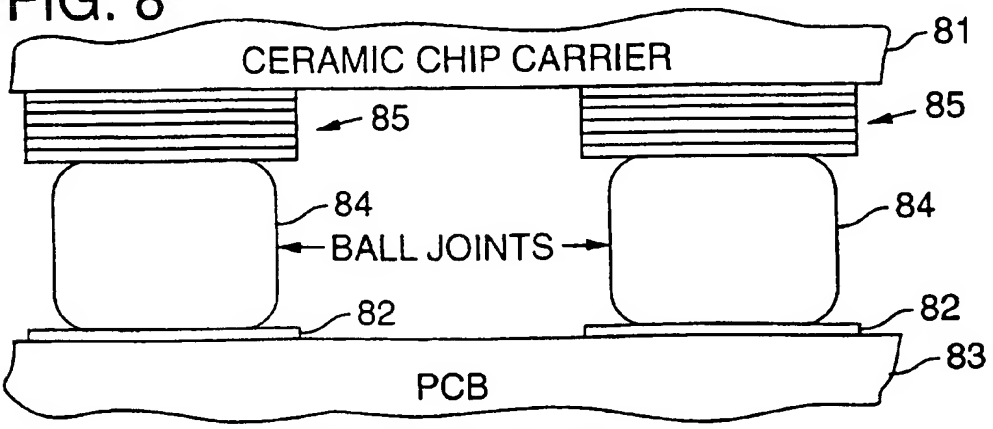


FIG. 8



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/07155

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :Please See Extra Sheet.
US CL : 257/ 736-738, 751, 762, 772, 779; 437/180, 183, 190
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/ 736-738, 751, 762, 772, 779; 437/180, 183, 190

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 87/00686 A (OSAKI ET AL.) 29 JANUARY 1987 (29/01/87), FIGURE 7, PAGE 9, LINES 1+.	1, 2, 4, 6-8
Y		3, 5, 9-14, 19, 20
Y	US 5,130,779 A (AGARWALA ET AL.) 14 JULY 1992 (14/07/92), FIGURE 4.	1-20
A	US 5,449,955 A (DEBIEC ET AL.) 12 SEPTEMBER, 1995 (12/09/95), FIGURE 3.	1-20
A	JP 6-84916 A (YANAGIHARA) 25 MARCH, 1994 (25/03/94), FIGURE 2.	1, 2,7-9

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 30 JUNE 1997	Date of mailing of the international search report 28 JUL 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer JIHAN B. CLARK Telephone No. (703) 308-4857

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/07155

A. CLASSIFICATION OF SUBJECT MATTER:
IPC (6):

H01L 21/44, 23/48, 23/52, 29/40

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

Group I, claim(s)1-10, drawn to a structure of a semiconductor device. (257/737)
Group II, claim(s) 11-20, drawn to the method for making the device. (437/183)
The inventions listed as Groups I and II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: group I, claims 1-10, lacks electroplating.